

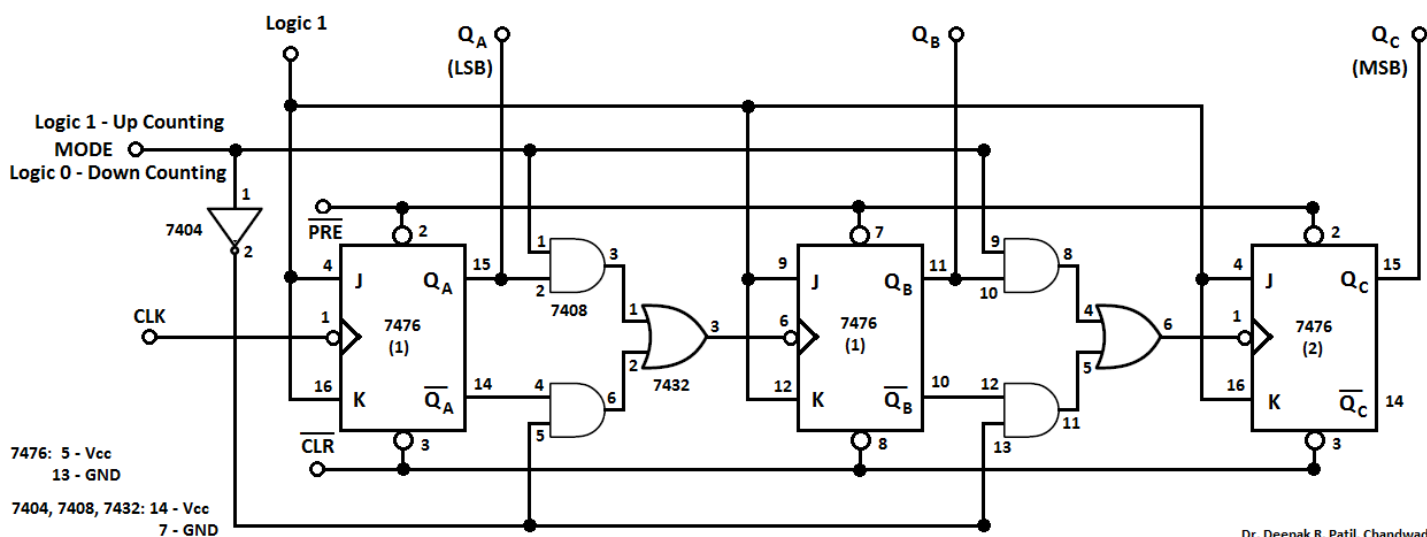
Title: 3 bit asynchronous Up/Down counter using flip flops.

Aim: To study 3 bit asynchronous Up/Down counter using flip flops.

Components: IC 7476 (-Ve edge triggered Dual J-K Flip-Flops), IC 7408 (Quad 2-input AND gates), IC 7432 (Quad 2-input OR gates), IC 7404 (Hex Inverters), LEDs, Resistor (220 Ω).

Equipment's and Miscellaneous: Regulated DC power supply (0-25V), DMM, Breadboard, Connecting wires etc.

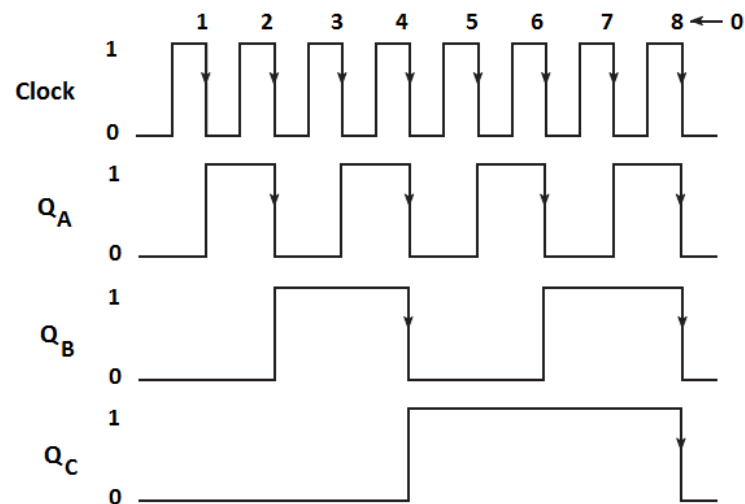
Circuit Diagram:



Note: Connect series combination of 220Ω resistor and LED between output and ground to see output.

Observation Table:

Up Counter				Down Counter			
Clock Input	Output			Clock Input	Output		
Count	QC	QB	QA	Count	QC	QB	QA
0	0	0	0	7	1	1	1
1	0	0	1	6	1	1	0
2	0	1	0	5	1	0	1
3	0	1	1	4	1	0	0
4	1	0	0	3	0	1	1
5	1	0	1	2	0	1	0
6	1	1	0	1	0	0	1
7	1	1	1	0	0	0	0

Timing Diagram:**A. Up Counter:**

Dr. Deepak R. Patil, Chandwad.

B. Down Counter: *(Draw the timing diagram for down counter in Practical Sheet)***Result:**

3 bit asynchronous Up/Down counter is studied and verified its truth table.

(Do not write on Practical Sheet)

Precautions:

1. Always connect ground first and then connect Vcc.
2. The kit should be off before changing the connections.
3. Switch off the kit after the experiment.

Procedure:**A. For Up Counting:**

4. Connect the circuit as shown in the diagram.
5. Connect \overline{PRE} input to the logic 1 i.e. +5V.
6. Connect \overline{CLR} input to the logic 0 i.e. 0V or ground to reset counter.
7. Connect \overline{CLR} input to the logic 1.
8. Connect Mode input to logic 1 for Up counting.
9. Apply the clock pulse to CLK input.
10. Observe the output and verify the observation table.

B. For Down Counting:

1. Connect the circuit as shown in the diagram.
2. Connect \overline{CLR} input to the logic 1 i.e. +5V.
3. Connect \overline{PRE} input to the logic 0 i.e. 0V or ground to set counter.
4. Connect \overline{PRE} input to the logic 1.
5. Connect Mode input to logic 0 for Down counting.
6. Apply the clock pulse to CLK input.
7. Observe the output and verify the observation table.