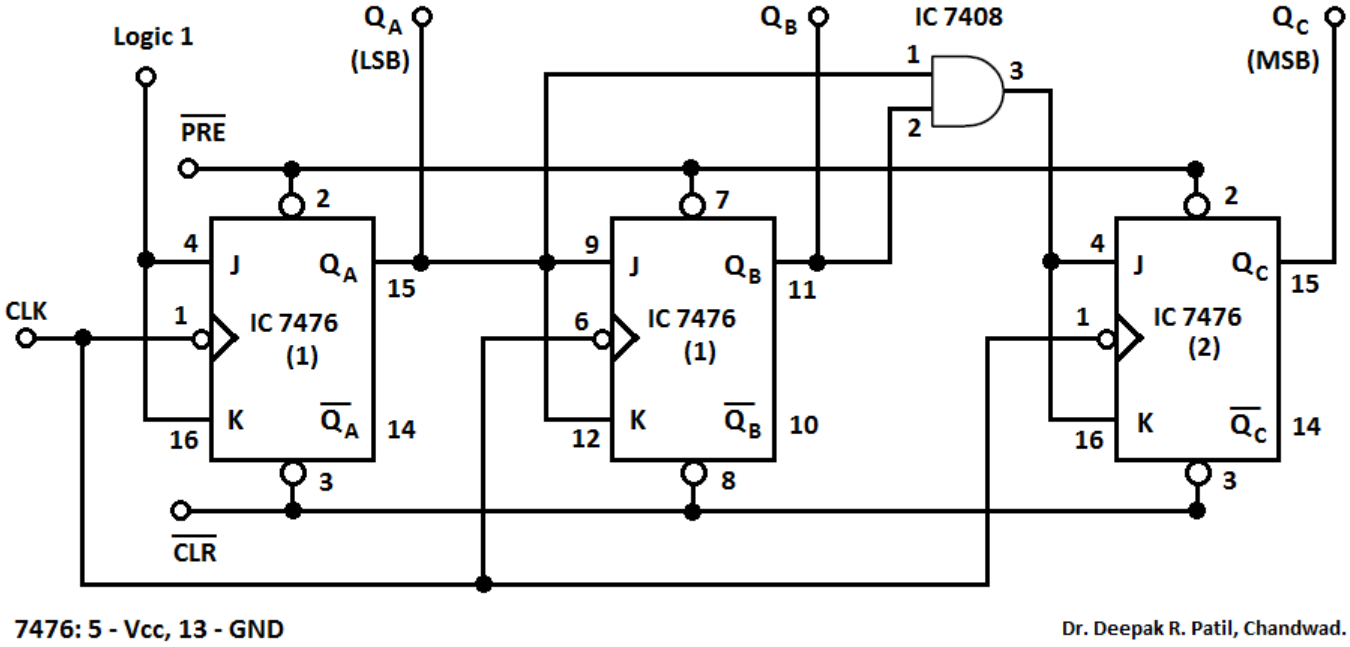
Title: 3-bit Synchronous Counter using Flip-Flops.

Aim: To study 3 bit synchronous counter (Up-Counter) using flip flops.

Components: IC 74LS76A (-Ve edge triggered Dual J-K Flip-Flops), IC 7408 (Dual I/P Quad AND gates).

Equipment's & Miscellaneous: Regulated DC power supply (0-25V), DMM, Breadboard, Connecting wires etc.

Circuit Diagram:



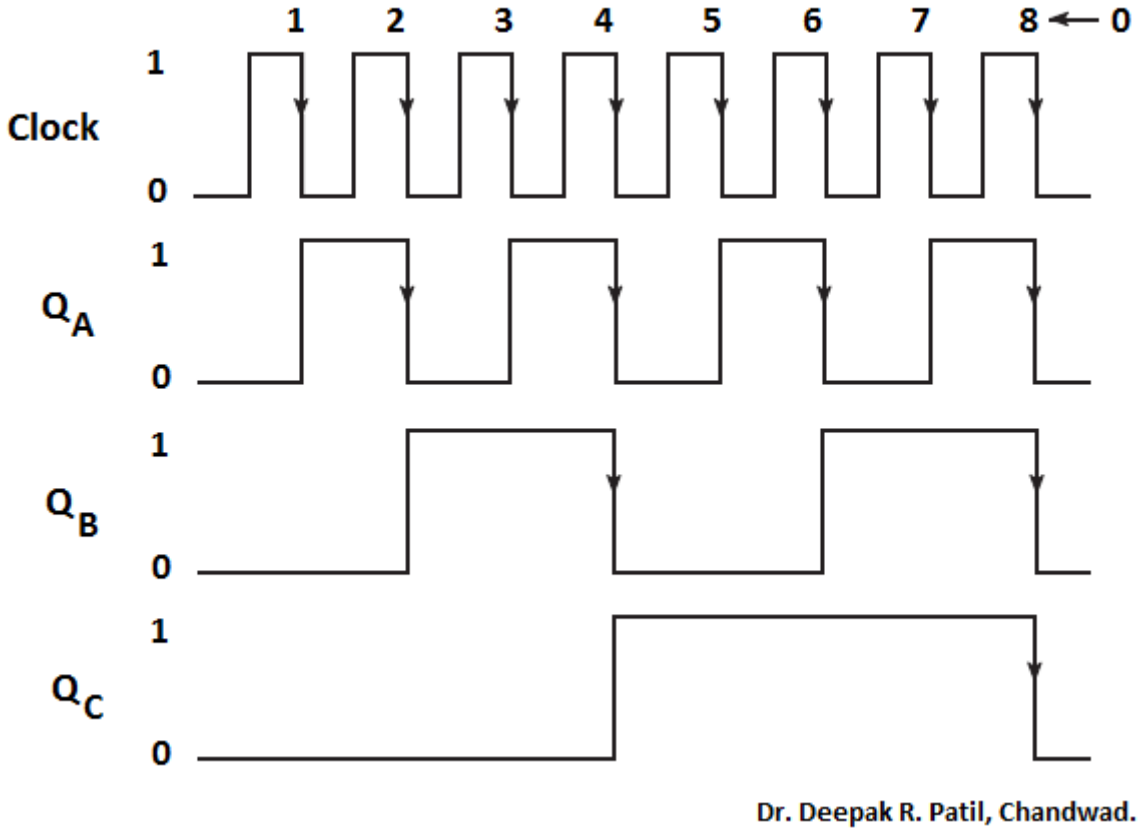
Note: 1. *Connect series combination of 220Ω resistor and LED between output and ground to see output.*

2. *IC 7473 (Dual JK flip-flop with reset; negative-edge trigger) can also use instead of IC 74LS76A.*

Observation Table:

Clock Input	Output		
Count	Q_C (2^2)	Q_B (2^1)	Q_A (2^0)
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Timing Diagram:



Result:

3 bit synchronous counter is studied and verified its truth table.

(Do not write on Practical Sheet)

Precautions:

1. Always connect ground first and then connect Vcc.
2. The kit should be off before changing the connections.
3. Switch off the kit after the experiment.

Procedure:

1. Connect the circuit as shown in the diagram.
2. Connect $\overline{PRE}$ input to the logic 1 i.e. +5V.
3. Connect $\overline{CLR}$ input to the logic 0 i.e. 0V or ground to reset counter.
4. Connect $\overline{CLR}$ input to the logic 1.
5. Apply the clock pulse to CLK input.
6. Observe the output and verify the observation table.